Section 5.1: Device Structure and Physical Operation

5.1
An NMOS transistor is fabricated in a 0.13-µm CMOS process with \(L = 1.5L_{\text{min}}\) and \(W = 1.3\ \mu m\). The process technology is specified to have \(t_{\text{ox}} = 2.7\ \text{nm}\), \(\mu_n = 400\ \text{cm}^2/\text{V} \cdot \text{s}\), and \(V_m = 0.4\ \text{V}\).

(a) Find \(C_{\text{ox}}, k_n',\) and \(k_n\).

(b) Find the overdrive voltage \(V_{OV}\) and the minimum value of \(V_{DS}\) required to operate the transistor in saturation at a current \(I_D = 100\ \mu\text{A}\). What gate-to-source voltage is required?

(c) If \(V_{DS}\) is very small, what values of \(V_{OV}\) and \(V_{GS}\) are required to operate the MOSFET as a 2-kΩ resistance? If \(V_{GS}\) is doubled, what \(r_{DS}\) results? If \(V_{GS}\) is reduced, at what value does \(r_{DS}\) become infinite?

Section 5.2: Current–Voltage Characteristics

5.2
An NMOS transistor fabricated in a 0.13-µm process has \(L = 0.2\ \mu m\) and \(W = 2\ \mu m\). The process technology has \(C_{\text{ox}} = 12.8\ \text{fF}/\mu\text{m}^2\), \(\mu_n = 450\ \text{cm}^2/\text{V} \cdot \text{s}\), and \(V_m = 0.4\ \text{V}\). Neglect the channel-length modulation effect.

(a) If the transistor is to operate at the edge of the saturation region with \(I_D = 100\ \mu\text{A}\), find the values required of \(V_{GS}\) and \(V_{DS}\).

(b) If \(V_{GS}\) is kept constant at the value found in (a) while \(V_{DS}\) is changed, find \(I_D\) that results at \(V_{DS}\) equal to half the value in (a) and at \(V_{DS}\) equal to 0.1 the value in (a).

(c) To investigate the operation of the MOSFET as a linear amplifier, let the operating point be at \(V_{GS} = 0.6\ \text{V}\) and \(V_{DS} = 0.3\ \text{V}\). Find the change in \(i_D\) for \(v_{GS}\) changing from 0.6 V by +10 mV and by −10 mV. Comment.

5.3
![Figure 5.3.1](image)

An NMOS transistor fabricated in a process for which the process transconductance parameter is 400 µA/V² has its gate and drain connected together. The resulting two-terminal device is fed with a current source \(I\) as shown in Fig. 5.3.1. With \(I = 40\ \mu\text{A}\), the voltage across the device is measured to be 0.6 V. When \(I\) is increased to 90 µA, the voltage increases to 0.7 V. Find \(V_i\) and \(W/L\) of the transistor. Ignore channel-length modulation.

5.4
An NMOS transistor for which \(k_n = 4\ \text{mA/V}^2\) and \(V_i = 0.35\ \text{V}\) is operated with \(V_{GS} = V_{DS} = 0.6\ \text{V}\). What current results? To what value can \(V_{DS}\) be reduced while maintaining the current unchanged? If the transistor is replaced with another fabricated in the same technology but
with twice the width, what current results? For each of the two transistors when operated at small \( V_{DS} \), what is the range of linear resistance \( r_{DS} \) obtained when \( V_{GS} \) is varied over the range 0.5 V to 1 V? Neglect channel-length modulation.

**5.5**

An NMOS transistor is fabricated in a 0.13-\(\mu\)m process having \( k_n' = 500 \mu A/V^2 \), and \( V_A' = 5 V/\mu m \).

(a) If \( L = 0.26 \mu m \) and \( W = 2.6 \mu m \), find \( V_A \) and \( \lambda \).

(b) If the device is operated at \( V_{OL} = 0.2 V \) and \( V_{DS} = 0.65 V \), find \( I_D \).

(c) Find \( r_o \) at the operating point specified in (b).

(d) If \( V_{DS} \) is increased to 1.3 V, what is the corresponding change in \( I_D \)? Do this two ways: using the expression for \( I_D \) and using \( r_o \). Compare the results obtained.

**5.6**

The PMOS transistor in Fig. 5.6.1 has \( V_{pp} = -0.5 V, k_p' = 100 \mu A/V^2 \), and \( W/L = 10 \).

(a) Find the range of \( v_G \) for which the transistor conducts.

(b) In terms of \( v_G \), find the range of \( v_D \) for which the transistor operates in the triode region.

(c) In terms of \( v_G \), find the range of \( v_D \) for which the transistor operates in saturation.

(d) Find the value of \( v_G \) and the range of \( v_D \) for which the transistor operates in saturation with \( I_D = 20 \mu A \). Assume \( \lambda = 0 \).

(e) If \( |\lambda| = 0.2 V^{-1} \), find \( r_o \) at the operating point in (d).

(f) For \( V_{OL} \) equal to that in (d) and \( |\lambda| = 0.2 V^{-1} \), find the value of \( I_D \) at \( V_D = 1 V \) and at \( V_D = 0 V \). Use these values to calculate the output resistance \( r_o \) and compare the result to that found in (e).

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**Section 5.3: MOSFET Circuits at DC**

**D5.7**

The NMOS transistor in the circuit in Fig. 5.7.1 has \( V_{tn} = 0.5 V, k_n' = 400 \mu A/V^2 \), \( W/L = 10 \), and \( \lambda = 0 \).

(a) Design the circuit (i.e., find the required values for \( R_S \) and \( R_D \)) to obtain \( I_D = 180 \mu A \) and \( V_D = +0.5 V \). Find the voltage \( V_S \) that results.

(b) If \( R_S \) is replaced with a constant-current source \( I \) as shown in Fig. 5.7.2, what must the value of \( I \) be to obtain the same operating conditions as in (a)?

(c) What is the largest value to which \( R_D \) can be increased while the transistor remains in saturation?
The PMOS transistor in the circuit in Fig. 5.8.1 has $V_{tp} = -0.5\ \text{V}$, $k'_p = 100\ \mu\text{A/V}^2$, $W/L = 20$, and $\lambda = 0$.

(a) Find $R_S$ and $R_D$ to obtain $I_D = 0.1\ \text{mA}$ and $V_D = 0\ \text{V}$.

(b) What is the largest $R_D$ for which the transistor remains in saturation. At this value of $R_D$, what is the voltage at the drain, $V_D$?

The NMOS transistor in the circuit in Fig. 5.9.1 has $V_t = 0.5\ \text{V}$, $k_n = 10\ \text{mA/V}^2$, and $\lambda = 0$. Analyze the circuit to determine the currents through all branches and to find the voltages at all nodes.

For the circuit in Fig. 5.10.1, the NMOS transistor has $V_m = 0.5\ \text{V}$, $k_n = 10\ \text{mA/V}^2$, and $\lambda = 0$, and the PMOS transistor has $V_{tp} = -0.5\ \text{V}$, $k_p = 12.5\ \text{mA/V}^2$, and $|\lambda_p| = 0$. Observe that $Q_1$ and its surrounding circuit is the same as the circuit analyzed in Problem 5.9 (Fig. 5.9.1), and you may use the results found in the solution to that problem here. Analyze the circuit to determine the currents in all branches and the voltages at all nodes.

The NMOS transistor in the circuit in Fig. 5.11.1 has $V_t = 0.5\ \text{V}$, $k_n = 4\ \text{mA/V}^2$, and $\lambda = 0$. Design the circuit in Fig. 5.11.1 to obtain $I = 1\ \mu\text{A}$, $I_D = 0.5\ \text{mA}$, $V_S = 2\ \text{V}$, and $V_D = 5\ \text{V}$. The NMOS transistor has $V_t = 0.5\ \text{V}$, $k_n = 4\ \text{mA/V}^2$, and $\lambda = 0$. 
The transistors in the circuits of Fig. 5.12.1 have $|V_t| = 0.5 \text{ V}$, $k_n = k_p = 20 \text{ mA/V}^2$, and $\lambda = 0$. Also, $I = 0.9 \text{ mA}$. For each circuit find $v_O$ as a function of $v_I$ assuming the transistors are operating in saturation. In each case find the allowable ranges of $v_O$ and $v_I$. Assume that the minimum voltage $V_{CS}$ required across each current source is 0.3 V.
5 MOS Field-Effect Transistors (MOSFETs)

5.1
(a) 
\[ L = 1.5L_{\text{min}} = 1.5 \times 0.13 = 0.195 \, \mu\text{m} \]
\[ C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{\ell_{\text{ox}}} \]
where
\[ \epsilon_{\text{ox}} = 3.9 \epsilon_0 = 3.9 \times 8.854 \times 10^{-12} \]
\[ = 3.45 \times 10^{-11} \, \text{F/m} \]
\[ C_{\text{ox}} = \frac{3.45 \times 10^{-11} \, \text{F/m}}{2.7 \times 10^{-9} \, \text{m}} \]
\[ = 1.28 \times 10^{-2} \, \text{F/\mu m} \]
\[ = 1.28 \times 10^{-2} \times 10^{15} \times 10^{-12} \, \text{fF/\mu m}^2 \]
\[ = 12.8 \, \text{fF/\mu m}^2 \]
\[ k_n = \mu_n C_{\text{ox}} \]
\[ = 400 \, \text{cm}^2/\text{V.s} \times 12.8 \, (\text{fF/\mu m}^2) \]
\[ = 400 \times 10^8 \, (\mu\text{m}^2/\text{V.s}) \times 12.8 \times 10^{-15} \, (\text{F/\mu m}^2) \]
\[ = 512 \times 10^{-6} \, (\text{F/V.s}) = 512 \times 10^{-6} \, (\text{A/V}^2) \]
\[ = 512 \, \mu\text{A/V}^2 \]
\[ k_n = k'_n \, (W/L) \]
\[ = 512 \times \frac{1.3}{0.195} = 3413 \, \mu\text{A/V}^2 \]
\[ k_n = 3.413 \, \text{mA/V}^2 \]

(b) When the MOSFET operates in saturation, we have
\[ I_D = \frac{1}{2} k_n V_{\text{OV}}^2 \]
Thus,
\[ 100 = \frac{1}{2} \times 3413 \times V_{\text{OV}}^2 \]
\[ \Rightarrow V_{\text{OV}} = 0.24 \, \text{V} \]

To operate in saturation, \( V_{\text{DS}} \) must at least be equal to \( V_{\text{OV}} \), thus
\[ V_{\text{DSmin}} = 0.24 \, \text{V} \]
The gate-to-source voltage is
\[ V_{\text{GS}} = V_{\text{in}} + V_{\text{OV}} = 0.4 + 0.24 = 0.64 \, \text{V} \]

(c) When \( V_{\text{DS}} \) is small,
\[ I_D \simeq k_n V_{\text{OV}} V_{\text{DS}} \]
and
\[ r_{\text{DS}} \equiv \frac{V_{\text{DS}}}{I_D} = 1/k_n V_{\text{OV}} \]
Thus, for \( r_{\text{DS}} = 2 \, \text{k}\Omega \),
\[ 2 \times 10^3 = \frac{1}{3.413 \times 10^{-3} \, V_{\text{OV}}} \]
\[ \Rightarrow V_{\text{OV}} = 0.15 \, \text{V} \]
and, correspondingly,
\[ V_{\text{GS}} = 0.4 + 0.15 = 0.55 \, \text{V} \]
If \( V_{\text{GS}} \) is doubled, we obtain
\[ V_{\text{GS}} = 2 \times 0.55 = 1.1 \, \text{V} \]
and
\[ V_{\text{OV}} = 1.1 - 0.4 = 0.7 \, \text{V} \]
Thus, correspondingly, \( r_{\text{DS}} \) becomes
\[ r_{\text{DS}} = \frac{1}{k_n V_{\text{OV}}} = \frac{1}{3.413 \times 10^{-3} \times 0.7} \]
\[ = 418.6 \, \Omega \]
As \( V_{GS} \) is reduced, \( r_{DS} \) increases, becoming infinite when the channel disappears, which occurs as \( V_{OV} \) reaches zero or, correspondingly,

\[ V_{GS} = V_m = 0.4 \text{ V} \]

### 5.2

(a) When the transistor operates in saturation, we obtain

\[ I_D = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right) V_{OV}^2 \]

where

\[ \mu_n C_{ox} = 450 \text{ (cm}^2 \text{/V-s)} \times 12.8 \text{ (fF/\mu m}^2 \text{)} \]

\[ = 450 \times 10^6 (\text{um}^2 \text{/V-s}) \times 12.8 \times 10^{-15} (\text{F/\mu m}^2) \]

\[ = 576 \times 10^{-6} (\text{F/V-s}) \]

\[ = 576 \text{ \mu A/V}^2 \]

To obtain \( I_D = 100 \text{ \mu A} \), \( V_{OV} \) can be found from

\[ 100 = \frac{1}{2} \times 576 \times \frac{2 \text{ \mu m}}{0.2 \text{ \mu m}} \times V_{OV}^2 \]

\[ \Rightarrow V_{OV} = 0.186 \text{ V} \]

Correspondingly,

\[ V_{GS} = V_m + V_{OV} = 0.4 + 0.186 = 0.586 \text{ V} \]

At the edge of saturation,

\[ V_{DS} = V_{DS_{min}} = V_{OV} = 0.186 \text{ V} \]

(b) If \( V_{DS} \) is lowered below \( V_{DS_{min}} \), the transistor operates in the triode region, thus

\[ i_D = \mu_n C_{ox} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_m) V_{DS} - \frac{1}{2} v_{DS}^2 \right] \]

\[ = 576 \times \frac{2}{0.2} (0.186 v_{DS} - 0.5 v_{DS}^2) \]

For

\[ v_{DS} = 0.5 V_{DS_{min}} = 0.5 \times 0.186 = 0.093 \text{ V} \]

we obtain

\[ i_D = 576 \times 10 (0.186 \times 0.093 - 0.5 \times 0.093^2) \]

\[ = 74.7 \text{ \mu A} \]

(c) For \( V_{GS} = 0.6 \text{ V} \) (i.e., \( V_{OV} = 0.2 \text{ V} \)) and \( V_{DS} = 0.3 \text{ V} \), the MOSFET will be operating in saturation with

\[ I_D = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right) V_{OV}^2 \]

\[ = \frac{1}{2} \times 576 \times \frac{2}{0.2} \times 0.2^2 \]

\[ = 115.2 \text{ \mu A} \]

Now, if \( V_{GS} \) is increased by a 10-mV increment, then

\[ V_{GS} = 0.6 + 0.010 = 0.610 \text{ V} \]

and the current becomes

\[ i_D = \frac{1}{2} \times 576 \times \frac{2}{0.2} \times (0.610 - 0.4)^2 \]

\[ = 127 \text{ \mu A} \]

Thus, \( i_D \) increases by an increment

\[ \Delta i_D = 127 - 115.2 = 11.8 \text{ \mu A} \]

If \( V_{GS} \) is decreased by 10 mV, we obtain

\[ V_{GS} = 0.6 - 0.010 = 0.590 \text{ V} \]

and the current becomes

\[ i_D = \frac{1}{2} \times 576 \times \frac{2}{0.2} \times (0.590 - 0.4)^2 \]

\[ = 104 \text{ \mu A} \]

Thus, the change in \( i_D \) is

\[ \Delta i_D = 104 - 115.2 = -11.2 \text{ \mu A} \]

Observe that the incremental changes in \( i_D \) are almost equal, indicating that the operation is almost linear. Linearity improves if the incremental changes in \( V_{GS} \) are made smaller. (For instance, try \( \Delta V_{GS} = \pm 5 \text{ mV} \).)
Refer to Fig. 5.3.1 and observe that since $V_{DS} = V_{GS} = V_t + V_{OV}$, we have

$$V_{DS} > V_{OV}$$

and thus the MOSFET is operating in the saturation region. Thus, ignoring channel-length modulation, we can write

$$I_D = \frac{1}{2} k_n \frac{W}{L} (V_{GS} - V_t)^2$$

Substituting the given data, we obtain

$$40 = \frac{1}{2} \times 400 \times \left(\frac{W}{L}\right) (0.6 - V_t)^2$$

and

$$90 = \frac{1}{2} \times 400 \times \left(\frac{W}{L}\right) (0.7 - V_t)^2$$

Dividing Eq. (2) by Eq. (1), we obtain

$$\frac{9}{4} = \frac{(0.7 - V_t)^2}{(0.6 - V_t)^2}$$

$$\Rightarrow \frac{3}{2} = \frac{0.7 - V_t}{0.6 - V_t}$$

which results in

$$V_t = 0.4 \text{ V}$$

Substituting for $V_t$ into Eq. (1) gives

$$40 = 200 \times \left(\frac{W}{L}\right) \times 0.04$$

$$\Rightarrow \frac{W}{L} = 5$$

5.4

Operation with $V_{DS} = V_{GS} = V_t + V_{OV}$ means $V_{DS} > V_{OV}$ and thus the MOSFET is in the saturation region. Thus, neglecting channel-length modulation, we can write for $I_D$,

$$I_D = \frac{1}{2} k_n (V_{GS} - V_t)^2$$

$$= \frac{1}{2} \times 4 \times (0.6 - 0.35)^2$$

$$= 0.125 \text{ mA}$$

The voltage $V_{DS}$ can be reduced to a value equal to $V_{OV}$ while the MOSFET remains in the saturation region, that is,

$$V_{DS_{\text{min}}} = 0.6 - 0.35 = 0.25 \text{ V}$$

A transistor having twice the value of $W$ will have twice the value of $k_n$ and thus the current will be twice as large, that is,

$$I_D = 2 \times 0.125 = 0.25 \text{ mA}$$

The linear resistance $r_{DS}$ is given by

$$r_{DS} = \frac{1}{k_n (V_{GS} - V_t)}$$

With $V_t = 0.35 \text{ V}$ and with $V_{GS}$ varying over the range $0.5 \text{ V}$ to $1 \text{ V}$, $r_{DS}$ will vary over the range

$$r_{DS} = \frac{1}{0.15 k_n} \text{ to } \frac{1}{0.65 k_n}$$

For the first device with $k_n = 4 \text{ mA/V}$, $r_{DS}$ will vary over the range

$$r_{DS} = \frac{1}{0.15 \times 4} = 1.67 \text{ k}\Omega$$

to

$$r_{DS} = \frac{1}{0.65 \times 4} = 0.38 \text{ k}\Omega$$

The wider device has $k_n = 8 \text{ mA/V}$ and thus its $r_{DS}$ will vary over the range

$$r_{DS} = 0.833 \text{ k}\Omega \text{ to } 0.192 \text{ k}\Omega$$
5.5
(a)\[ V_A = V'_A L = 5 \times 0.26 = 1.3 \text{ V} \]
\[ \lambda = \frac{1}{V_A} = \frac{1}{1.3} = 0.77 \text{ V}^{-1} \]

(b) Since \( V_{DS} = 0.65 \text{ V} \) is greater than \( V_{OV} \), the NMOS transistor is operating in saturation. Thus,
\[ I_D = \frac{1}{2} k'_n \left( \frac{W}{L} \right) V_{OV}^2 \left( 1 + \lambda V_{DS} \right) \]
\[ = \frac{1}{2} \times 500 \times \frac{2.6}{0.26} \times 0.2^2 \left( 1 + 0.77 \times 0.65 \right) \]
\[ = 150 \text{ mA} \]

(c) \[ r_o = \frac{V_A}{I_D} \]
where \( I'_D \) is the drain current without taking channel-length modulation into account, thus
\[ I'_D = \frac{1}{2} k'_n \left( \frac{W}{L} \right) V_{OV}^2 \]
\[ = \frac{1}{2} \times 500 \times \frac{2.6}{0.26} \times 0.2^2 \]
\[ = 100 \text{ mA} \]

Hence,
\[ r_o = \frac{1.3 \text{ V}}{100 \text{ mA}} = \frac{1.3 \text{ V}}{0.1 \text{ mA}} = 13 \text{ k}\Omega \]

(d) If \( V_{DS} \) is increased to 1.3 V, \( I_D \) becomes
\[ I_D = \frac{1}{2} \times 500 \times \frac{2.6}{0.26} \times 0.2^2 \left( 1 + 0.77 \times 1.3 \right) \]
\[ = 200 \text{ mA} \]

That is, \( I_D \) increases by 50 mA. Alternatively, we can use \( r_o \) to determine the increase in \( I_D \) as
\[ \Delta I_D = \frac{\Delta V_{DS}}{r_o} \]
\[ = \frac{0.65 \text{ V}}{13 \text{ k}\Omega} = 0.05 \text{ mA} = 50 \text{ mA} \]

which is identical to the result obtained directly.

5.6
(a) For the transistor to conduct, \( v_G \) must be lower than \( v_S \) by at least \( |V_{tp}| \), that is, by 0.5 V. Thus, the transistor conducts for \( v_G \leq 1.8 - 0.5 \), or \( v_G \leq 1.3 \text{ V} \).

(b) For the transistor to operate in the triode region, the drain voltage must be higher than the gate voltage by at least \( |V_{tp}| \) volts, thus
\[ v_D \geq v_G + 0.5 \text{ V} \]

(c) For the transistor to operate in the saturation region, the drain voltage cannot exceed the gate voltage by more than \( |V_{tp}| \), that is,
\[ v_D \leq v_G + 0.5 \text{ V} \]

(d) When the transistor is operating in saturation, we obtain
\[ I_D = \frac{1}{2} k'_p \left( \frac{W}{L} \right) |V_{OV}|^2 \]

Substituting the given values, we obtain
\[ 20 = \frac{1}{2} \times 100 \times 10 |V_{OV}|^2 \]
\[ \Rightarrow |V_{OV}| = 0.2 \text{ V} \]

which is obtained when
\[ v_G = V_{DD} - V_{SG} \]
\[ = 1.8 - (|V_{tp}| + |V_{OV}|) \]
\[ = 1.8 - (0.5 + 0.2) = 1.1 \text{ V} \]

For this value of \( v_G \), the range that \( v_D \) is allowed to have while the transistor remains in saturation is
\[ v_D \leq v_G + |V_{tp}| \]
that is,
\[ v_D \leq 1.6 \text{ V} \]

(e) 
\[ r_o = \frac{|V_A|}{I_D} = \frac{1}{|\lambda|I_D} \]

where \( I'_D \) is the value of \( I_D \) without channel-length modulation taken into account, that is,
\[ I'_D = \frac{1}{2} k'_n \left( \frac{W}{L} \right) V^2_{OV} (1 + |\lambda|V_{SD}) \]

\[ = \frac{1}{2} \times 100 \times 10 \times 0.2^2 = 20 \mu\text{A} \]

Thus,
\[ r_o = \frac{1}{0.2 \times 20} = 0.25 \text{ M}\Omega \]

(f) 
\[ I_D = \frac{1}{2} k'_p \left( \frac{W}{L} \right) V^2_{OV} (1 + |\lambda|V_{SD}) \]

At \( V_D = 1 \text{ V} \), we have \( V_{SD} = 1.8 - 1 = 0.8 \text{ V} \), and
\[ I_D = \frac{1}{2} \times 100 \times 10 \times 0.2^2 (1 + 0.2 \times 0.8) = 23.2 \mu\text{A}. \]

At \( V_D = 0 \text{ V} \), we get \( V_{SD} = 1.8 - 0 = 1.8 \text{ V} \), and
\[ I_D = \frac{1}{2} \times 100 \times 10 \times 0.2^2 (1 + 0.2 \times 1.8) = 27.2 \mu\text{A} \]

Thus, for
\[ \Delta V_{SD} = 1.8 - 0.8 = 1 \text{ V}, \]

the current changes by
\[ \Delta I_D = 27.2 - 23.2 = 4 \mu\text{A} \]

indicating that the output resistance \( r_o \) is
\[ r_o = \frac{\Delta V_D}{\Delta I_D} = \frac{1 \text{ V}}{4 \mu\text{A}} = 0.25 \text{ M}\Omega \]

which is the same value found in (e).
Finally, the value of $R_D$ can be found from

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{1 - 0.5}{0.18 \text{ mA}} = 2.78 \, \text{k}\Omega$$

(c) Refer to Fig. 5.7.1. As $R_D$ is increased, $V_D$ decreases as

$$V_D = 1 - I_D R_D = 1 - 0.18 R_D$$

Eventually, $V_D$ falls below $V_G$ by $V_m$ at which point the transistor leaves the saturation region and enters the triode region. This occurs at

$$V_D = V_G - V_m = 0 - 0.5 = -0.5 \, \text{V}$$

The corresponding value of $R_D$ can be found from

$$-0.5 = 1 - 0.18 \times R_D \Rightarrow R_D = 8.33 \, \text{k}\Omega$$

5.8

(a) With $V_D = 0 \, \text{V}$, the transistor will be operating in the saturation region since $V_D = V_G$. Thus,

$$I_D = \frac{1}{2} k' p \left( \frac{W}{L} \right) |V_{OV}|^2$$

where we have taken into account that $\lambda = 0$ as stated. To obtain $I_D = 0.1 \, \text{mA} = 100 \, \mu\text{A}$, the required value of $|V_{OV}|$ can be found as follows:

$$100 = \frac{1}{2} \times 100 \times 20 |V_{OV}|^2 \Rightarrow |V_{OV}| = 0.316 \, \text{V}$$
The value of $V_{SG}$ can now be found as

$$V_{SG} = |V_Tp| + |V_{OV}| = 0.5 + 0.316 = 0.816 \text{ V}$$

Thus,

$$V_S = V_{SG} = 0.816 \text{ V}$$

The required value of $R_S$ can be determined from

$$R_S = \frac{V_{DD} - V_S}{ID}$$

$$= \frac{1 - 0.816}{0.1} = 1.84 \text{ k}\Omega$$

Finally, the required value of $R_D$ can be found from

$$R_D = \frac{V_D - (V_{SS})}{ID}$$

$$= \frac{0 - (-1)}{0.1} = 10 \text{ k}\Omega$$

The designed circuit with component values and current and voltage values is shown in Figure 5.8.2. The reader can check the calculations directly on the circuit diagram.

To obtain this value of $V_D$, $R_D$ must be increased to

$$R_D = \frac{V_{D_{\text{max}}} - (-1)}{0.1 \text{ mA}} = \frac{0.5 + 1}{0.1} = 15 \text{ k}\Omega$$

5.9

The current $I$ through the voltage divider $R_{G1}$–$R_{G2}$ can be found as

$$I = \frac{V_{DD}}{R_{G1} + R_{G2}}$$

$$= \frac{5 \text{ V}}{3 \text{ M}\Omega + 2 \text{ M}\Omega} = \frac{5 \text{ V}}{5 \text{ M}\Omega} = 1 \mu\text{A}$$

The voltage $V_G$ at the gate can now be found as

$$V_G = IR_{G2} = 1 \mu\text{A} \times 2 \text{ M}\Omega = 2 \text{ V}$$

The voltage $V_S$ is given by

$$V_S = V_G - V_{GS} = V_G - (V_t + V_{OV})$$

$$= 2 - (0.5 + V_{OV})$$

But $V_S$ can be expressed in terms of $I_D$ as

$$V_S = I_D R_S = I_D \times 6.5 = 6.5 I_D$$

Thus,

$$6.5 I_D = 1.5 - V_{OV}$$  \hspace{1cm} (2)$$

(b) Refer to Figure 5.8.1. The transistor remains in saturation as long as $V_D$ does not increase above $V_G$ by more than $|V_{Tp}|$. Since $V_G = 0$ and $|V_{Tp}| = 0.5 \text{ V}$, the maximum allowable value of $V_D$ is

$$V_{D_{\text{max}}} = +0.5 \text{ V}$$
We do not know whether the transistor is operating in the saturation region or in the triode region. Therefore, we must make an assumption about the region of operation, complete the analysis, and then use the results obtained to check the validity of our assumption. If our assumption proves valid, our work is done. Otherwise, we must redo the analysis assuming the other mode of operation. Since the $i-v$ relationships that describe the saturation-region operation are simpler than those that apply in the triode region, we normally assume operation in the saturation region, unless of course there is an indication of triode-mode operation.

Assuming that the transistor in the circuit of Figure 5.9.1 is operating in saturation, we can write

$$I_D = \frac{1}{2} \cdot k_n V_{OV}^2 = \frac{1}{2} \times 10 \cdot V_{OV}^2 = 5V_{OV}^2$$

Substituting for $I_D$ from Eq. (3) into Eq. (2) gives

$$6.5 \times 5V_{OV}^2 = 1.5 - V_{OV}$$

which can be rearranged into the form

$$32.5V_{OV}^2 + V_{OV} - 1.5 = 0$$

Solving this quadratic equation yields

$$V_{OV} = 0.2 \text{ V or } -0.23 \text{ V}$$

Obviously, the negative value is physically meaningless and can be discarded. Thus,

$$V_{OV} = 0.2 \text{ V}$$

and

$$I_D = 5V_{OV}^2 = 5 \times 0.2^2 = 0.2 \text{ mA}$$

We are now ready to check the validity of our assumption of saturation mode operation. Referring to the circuit in Figure 5.9.1, we can find the voltage $V_D$ as follows:

$$V_D = V_{DD} - I_D R_D$$

$$= 5 - 0.2 \times 12.5 = 2.5 \text{ V}$$

which is greater than $V_G$ (2 V), confirming that the transistor is operating in saturation, as assumed. Figure 5.9.2 shows the circuit together with the values of all node voltages and branch currents.

The reader is encouraged to check their results by doing a few calculations directly on the circuit.

5.10

From Fig. 5.10.1 in the problem statement we observe that transistor $Q_1$ together with its associated resistors is an identical circuit to that analyzed in the solution to Problem 5.9 (see Fig. 5.9.1). Since the gate terminal of $Q_2$ draws zero current, transistor $Q_2$ together with its associated resistances do not change the currents and voltages in $Q_1$ and its associated resistances. Thus, we need to only concern ourselves with the analysis of the part of the circuit shown in Figure 5.10.2, where $V_{GS}$ is found from

$$V_{G2} = V_{D1} = 2.5 \text{ V}$$

Figure 5.10.2
Since we do not know whether $Q_2$ is operating in saturation or in the triode region, we shall assume saturation-mode operation and, of course, we will have to check the validity of this assumption. We can now write

\[ I_{D2} = \frac{1}{2} k_p |V_{OV2}|^2 \]

\[ = \frac{1}{2} \times 12.5 |V_{OV2}|^2 \]

Thus,

\[ I_{D2} = 6.25 |V_{OV2}|^2, \text{ mA} \] (1)

Another relationship between $I_{D2}$ and $|V_{OV2}|$ can be obtained as follows:

\[ V_{S2} = V_{G2} + V_{SG2} \]

\[ = V_{G2} + (|V_{p}| + |V_{OV2}|) \]

\[ = 2.5 + 0.5 + |V_{OV2}| \]

\[ = 3 + |V_{OV2}| \]

But

\[ I_{D2} = \frac{V_{DD} - V_{S2}}{R_{S2}} \]

\[ = \frac{5 - (3 + |V_{OV2}|)}{7.2} \]

\[ I_{D2} = \frac{2 - |V_{OV2}|}{7.2}, \text{ mA} \] (2)

Equating $I_{D2}$ from Eqs. (1) and (2) results in

\[ 6.25 |V_{OV2}|^2 = \frac{2 - |V_{OV2}|}{7.2} \]

which can be rearranged into the form

\[ 45 |V_{OV2}|^2 + |V_{OV2}| - 2 = 0 \]

This quadratic equation can be solved to obtain

\[ |V_{OV2}| = 0.2 \text{ V or } -0.22 \text{ V} \]

Obviously, the negative solution is physically meaningless, thus

\[ |V_{OV2}| = 0.2 \text{ V} \]

and

\[ I_{D2} = 6.25 \times 0.2^2 = 0.25 \text{ mA} \]

We are now ready to check the validity of our assumption of saturation-mode operation. We can do this by finding $V_{D2}$:

\[ V_{D2} = I_{D2} R_{D2} = 0.25 \times 8 = 2 \text{ V} \]

which is lower than the voltage at the gate ($V_{G2} = 2.5$ V), confirming saturation-mode operation. The voltage $V_{S2}$ can be found as

\[ V_{S2} = V_{DD} - I_{D2} R_{S2} = 5 - 0.25 \times 7.2 = +3.2 \text{ V} \]

Finally, Fig. 5.10.3 shows the complete circuit with all currents and voltages. The values associated with $Q_1$ are those obtained in the solution for Problem 5.9. The reader is urged to make a few quick checks on the results displayed in Fig. 5.10.3.
Refer to Fig. 5.11.1. We assume that the transistor is operating in the saturation mode, thus

\[ I_D = \frac{1}{2} k_n V_{OV}^2 \]

where we have taken account of the stated value \( \lambda = 0 \). To obtain \( I_D = 0.5 \text{ mA} \), the required value of \( V_{OV} \) can be found from

\[ 0.5 = \frac{1}{2} \times 4 V_{OV}^2 \]

\[ \Rightarrow V_{OV} = 0.5 \text{ V} \]

Now, since

\[ V_{DS} = V_D - V_S = 5 - 2 = 3 \text{ V} \]

is greater than \( V_{OV} \), the MOSFET is operating in saturation, as assumed. The required value of \( R_S \) can be determined as follows:

\[ R_S = \frac{V_S}{I_D} = \frac{2}{0.5} = 4 \text{ k}\Omega \]

and the required value of \( R_D \) can be determined as follows:

\[ R_D = \frac{V_{DD} - V_D}{I_D} = \frac{10 - 5}{0.5} = 10 \text{ k}\Omega \]

The voltage at the gate \( V_G \) is found as

\[ V_G = V_{GS} + V_S \]

where

\[ V_{GS} = V_t + V_{OV} = 0.5 + 0.5 = 1 \text{ V} \]

Thus,

\[ V_G = 1 + 2 = 3 \text{ V} \]

The resistance \( R_{G1} \) can be found as follows:

\[ R_{G1} = \frac{V_{DD} - V_G}{I} = \frac{10 - 3}{1 \mu\text{A}} = 7 \text{ M}\Omega \]

and, finally, \( R_{G2} \) can be found as

\[ R_{G2} = \frac{V_G}{I} = \frac{3 \text{ V}}{1 \mu\text{A}} = 3 \text{ M}\Omega \]

The voltage at the gate \( V_G \) is found as

\[ V_G = V_{GS} + V_S \]

where

\[ V_{GS} = V_t + V_{OV} = 0.5 + 0.3 = 0.8 \text{ V} \]

Thus,

\[ v_O = v_I - V_{GS} \]

and \( V_{OV} \) can be found from

\[ I_D = I = \frac{1}{2} k_n V_{OV}^2 \]

Thus,

\[ 0.9 = \frac{1}{2} \times 20 V_{OV}^2 \]

\[ \Rightarrow V_{OV} = 0.3 \text{ V} \]

and

\[ V_{GS} = 0.5 + 0.3 = 0.8 \text{ V} \]

Thus,

\[ v_O = v_I - 0.8 \tag{1} \]

The highest value that \( v_O \) can have while the transistor remains in saturation is limited by the need to keep \( v_{DS} \) at least equal to \( V_{OV} \), thus

\[ v_{Omax} = 2.5 - V_{OV} = 2.2 \text{ V} \]

The lowest value that \( v_O \) can have is limited by the need to keep the voltage across the current source \( V_{CS} \) at least equal to 0.3 V, thus

\[ v_{Omin} = -2.5 + 0.3 = -2.2 \text{ V} \]

Thus, the allowable range of \( v_O \) is

\[ -2.2 \text{ V} \leq v_O \leq +2.2 \text{ V} \]
and the corresponding allowable range of \( v_I \) can be found using Eq. (1) as

\[-1.4 \, V \leq v_I \leq +3 \, V\]

(b)

Figure 5.12.1(b)

\[ v_O = v_I + V_{SG} \]

where

\[ V_{SG} = |V_I| + |V_{OV}| \]

and \( |V_{OV}| \) can be found from

\[ I_D = I = \frac{1}{2} k_p |V_{OV}|^2 \]
\[ 0.9 = \frac{1}{2} \times 20 |V_{OV}|^2 \]
\[ \Rightarrow |V_{OV}| = 0.3 \, V \]

Thus,

\[ V_{SG} = 0.5 + 0.3 = 0.8 \, V \]

and,

\[ v_O = v_I + 0.8 \]  \hspace{1cm} (2)

The highest value that \( v_O \) can have is limited by the need to keep the voltage \( V_{CS} \) across the current source to at least 0.3 V, thus

\[ v_{O_{\text{max}}} = 2.5 - 0.3 = 2.2 \, V \]

The lowest value that \( v_O \) can have is limited by the need to keep the voltage \( v_{SD} \) to a value at least equal to \( |V_{OV}| \), thus

\[ v_{O_{\text{min}}} = -2.5 + 0.3 = -2.2 \, V \]

Thus, the allowable range of \( v_O \) is

\[-2.2 \, V \leq v_O \leq +2.2 \, V\]

The corresponding range of \( v_I \) can be determined using Eq. (2) as

\[-3 \, V \leq v_I \leq +1.4 \, V\]

(c)

Figure 5.12.1(c)

From the results of (a) and (b), we know that

\[ V_{GS1} = V_{SG2} = 0.8 \, V \]

The voltage \( v_O \) can be found as follows:

\[ v_O = v_I - V_{GS1} + V_{GS2} \]
\[ = v_I - 0.8 + 0.8 \]

Thus,

\[ v_O = v_I \]  \hspace{1cm} (3)

The highest value of \( v_O \) is determined by the need to keep the voltage \( V_{CS} \) across the current source \( I \) of \( Q_2 \) at least equal to 0.3 V. Thus,

\[ v_{O_{\text{max}}} = 2.5 - 0.3 = +2.2 \, V \]

At this value, the voltage at the source of \( Q_1 \) is

\[ v_{S1} = 2.2 - 0.8 = +1.4 \, V \]

which is an allowed value as we determined in (a) above.
The lowest value of $v_O$ can be determined by the need to maintain a minimum $v_{SD}$ across $Q_2$ of value equal to $|V_{OP}| = 0.3$ V. This would imply that $v_O$ can be as low as $-2.5 + 0.3 = -2.2$ V. However, $v_O = -2.2$ V would require $v_{S1}$ to be $v_{S1} = -2.2 - V_{SG} = -2.2 - 0.8 = -3$ V, which is not within the allowable range for $v_{S1}$ [see (a) above]. It follows that the lowest allowable value of $v_O$ is determined by the lowest allowable value at the source of $Q_1$:

$$v_{O\text{min}} = v_{S1\text{min}} + V_{SG}$$
$$= -2.2 + 0.8$$
$$= -1.4 \text{ V}$$

Thus, the allowable range of $v_O$ is

$$-1.4 \text{ V} \leq v_O \leq +2.2 \text{ V}$$

and using Eq. (3), the allowable range of $v_I$ can be found as

$$-1.4 \text{ V} \leq v_I \leq +2.2 \text{ V}$$

Figure 5.12.1(d)

Following a procedure identical to that we used for (c) above, we can show that here

$$v_O = v_I$$

(4)

and that the allowable range at the output is

$$-2.2 \text{ V} \leq v_O \leq +1.4 \text{ V}$$

and at the input

$$-2.2 \text{ V} \leq v_I \leq +1.4 \text{ V}$$